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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,057	02/17/2004	Seong-jin Jang	5649-1204	9675

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,057	JANG, SEONG-JIN	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,12-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-14* is/are allowed.

6)☒ Claim(s) *1-3,5-8,16,17 and 20-22* is/are rejected.

7)☒ Claim(s) *4,9,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 8 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Song (U. S. PAT. 6,768,393).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In claim 1, Song teaches all claimed features in Fig. 2, a semiconductor device, comprising: an on-chip termination circuit that is configured to generate a variable resistance (41) to an input signal (10) based on at least one code signal (UPCODE); a reference voltage generator (42, 43) that is configured to generate a reference voltage (N3) based on the at least one code signal (UPCODE); and an input buffer (23) that is

configured to generate an internal signal (To 30) based on the input signal (10) from the on-chip terminal circuit and the reference voltage (N3).

In claim 8, Song further teaches in Fig. 2, the semiconductor device of Claim 1, wherein the reference voltage generator (located in 20) is configured to generate the reference voltage based on an external reference voltage signal (Rext) that is received from external to the semiconductor device.

Claim 16 corresponds to detailed circuitry already discussed similarly with regard to claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 5-7, 17 and 20-22 are rejected under 35 U.S.C. 103(a) as being obvious over Song in view of applicant's admitted prior art in Fig. 1.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In claim 2, Song teaches all claimed features of the semiconductor of claim 1; with the exception of teaching wherein the at least one code signal comprises a pull-up code signal and a pull-down code signal. However, the applicant's admitted prior art in Fig. 1 teaches the at least one code signal comprises a pull-up code signal (CD1) and a pull-down code signal (CD2), and wherein the on-chip termination circuit comprises; a pull-up termination resistor (RU) that is configured to have a variable resistance (arrow symbol) based on the pull-up code signal (CD1); and a pull-down termination resistor (RD) that is configured to have a variable resistance based on the pull-down code signal (CD2), wherein the pull-up termination resistor and the pull-down termination resistor are connected in series between a first power supply voltage (VDD) and a second power supply voltage (gnd), and wherein the input signal (112) is conducted through a connection node (IS1) between the pull-up termination resistor and the pull-down termination resistor.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Song with the teachings of the

applicant's admitted prior art to provide a circuit and method for calibrating resistors to have the same resistance as that of an external resistor irrespective of changes in process, voltage, or temperature.

In claim 3, Song further teaches the semiconductor of claim 2, wherein the reference voltage generator comprises: a first resistor (42) that is configured to have a variable resistance based on the pull-up code signal (UPCODE); and a second resistor (43) that is configured to have a variable resistance based on the pull- down code signal (DNCODE), wherein the first and second resistors are connected in series between the first power supply voltage (VDDQ) and the second power supply voltage (VSSQ), and wherein the reference voltage is generated at a node (N3) between the first and second resistors.

In claim 5, Song further teaches in Fig. 2, the semiconductor of claim 2 further comprising a calibration circuit (20) that is configured to generate the pull-up code signal (UPCODE) and the pull-down code signal (DNCODE) based on resistance of an external resistor (Rext) that is external to the semiconductor device.

In claim 6, Song teaches all claimed features the semiconductor device of Claim 1; with the exception of teaching wherein the on-chip termination circuit comprises a termination resistor that is configured to generate a variable resistance to the input signal based on a first code signal. However, the applicant's admitted prior art in Fig. 1 teaches wherein the on-chip termination circuit comprises a termination resistor (RU) that is configured to generate a variable resistance (arrow symbol) to the input signal (112) based on a first code signal (CD1).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of Song with the teachings of the applicant's admitted prior art to provide a circuit and method for calibrating resistors to have the same resistance as that of an external resistor irrespective of changes in process, voltage, or temperature.

In claim 7, the applicant's admitted prior art in Fig. 1 further teaches the semiconductor device of Claim 6, wherein the termination resistor is connected between a power supply voltage (VDD) and a node (IS1) through which the input signal (112) is conducted to the input buffer (231).

Claims 17 and 20-22 correspond to detailed circuitry already discussed similarly with regard to claims 1-3 and 5-8.

5. Claims 4, 9, 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 12-14 appear to comprise allowable subject maters.

Response to Arguments

7. The new ground(s) of rejection have been applied in light of the newly found reference of Song.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER